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2. 512K缓存使用主板上的 256K SRAM 及 256K的缓存模块没有 Tag SRAM 装置

SRAM	位置	类型	速度	电压
Tag SRAM	U10	32Kx8	15ns	5V I/O
Data SRAM (1 st 256KB)	U41, U43	2 片 32Kx32 pipelined burst SRAM	7ns (Clock to o/p valid)	3.3V I/O
Data RAM (2 nd 256KB)	DM1	256K Cache Module w/o Tag RAM	7ns (Clock to o/p valid)	3.3V I/O

JP16	JP50
2-3	1-2

4.2.3 外设设置

PS/2 鼠标设置

	JP31	JP32	JP33
有效	1-2 *	2-3 *	2-3 *
无效	2-3	1-2	1-2

Table of Contents

Chapter 1: System Overview

1.1	General Specification Overview	2
1.2	Central Processing Unit.....	5
1.3	External Cache Subsystem.....	5
1.4	DRAM Subsystem	6
1.5	PCI Bus	6
1.6	Universal Serial Bus.....	6
1.7	Super I/O Subsystem.....	7
1.8	Input/Output Subsystem.....	7
1.9	BIOS Subsystem	7

Chapter 2: Installation and Upgrade

2.1	CPU Installation.....	8
2.2	Fast Page mode / EDO DRAM Installation	9
2.3	Control of System Speed.....	11
2.4	Reset CMOS	11

Appendix-A: Connectors Pinout

A.1	Reset Connector (P1)	12
A.2	Turbo LED Connector (P2).....	12
A.3	Speaker Connector (P3)	12
A.4	Keylock Connector (P4).....	12
A.5	HD LED Connector (P5).....	13
A.6	External Battery Connector (P9).....	13
A.7	Sleep Switch (P10)	13
A.8	USB Connector (P24).....	13

CHAPTER 1

SYSTEM OVERVIEW

OCTEK RHINO 6VX is a powerful PC machine offering unparalleled performance. The advanced external cache system implemented meets the demand of the most memory-intensive applications today. The support of Synchronous Cache RAM (pipelined burst SRAM) and EDO DRAM results in better performance when compared with traditional asynchronous SRAM and Fast Page Mode DRAM. With the Pentium processor and a high bandwidth 32-bit PCI expansion bus, the I/O bottleneck that plagues most PC systems is now removed.

All of the I/O is integrated inside the mainboard to further facilitate system installation. The built-in IDE can support up to 4 fast Enhanced IDE devices whereas it can also support up to two floppy drives. The mainboard also includes two serial ports and one parallel port as the basic configuration for end user. All that is needed is just a VGA card plugged into a PCI or ISA slot to complete the whole system.

4.2 跳线设置

在下列表格中, 所有厂家设置均以 * 号标明

4.2.1 CPU有关设置

CPU电压选择

JP52	CPU 电压	CPU 种类
1-2	3.5V(VRE)	Cyrix 6x86, AMD K5
3-4*	3.3V	Intel P54C, P54CQS, P54CS,

注意: CPU的电压要正确设定, 否则会对CPU造成永久性的损坏

CPU 种类

JP4	JP5	JP8	JP9	JP10	CPU 时钟	CPU 种类
1-2	1-2	2-3	2-3	1-2	50MHz	Intel P54C-75
2-3	1-2	2-3	2-3	1-2		Cyrix 6x86-P120+ (100MHz)
1-2	1-2	2-3	2-3	1-2		AMD K5-PR75 (75MHz)
2-3	1-2	1-2	1-2	1-2	55MHz	Cyrix 6x86-P133+ (110MHz)
1-2	1-2	1-2	2-3	2-3	60MHz	Intel P54C-90
2-3	1-2	1-2	2-3	2-3		Intel P54C-120
2-3	2-3	1-2	2-3	2-3		Intel P54C-150
1-2	2-3	1-2	2-3	2-3		Intel P54C-180
2-3	1-2	1-2	2-3	2-3		Cyrix 6x86-P150+ (120MHz)
1-2	1-2	1-2	2-3	2-3		AMD K5-PR90 (90MHz)
1-2	1-2	1-2	2-3	2-3		AMD K5-PR120 (90MHz)
2-3	1-2	1-2	2-3	2-3		AMD K5-PR150 (120MHz)
1-2	1-2	2-3	1-2	2-3	66MHz	Intel P54C-100
2-3	1-2	2-3	1-2	2-3		Intel P54C-133
2-3	2-3	2-3	1-2	2-3		Intel P54C-166
1-2	2-3	2-3	1-2	2-3		Intel P54C-200
2-3	1-2	2-3	1-2	2-3		Cyrix 6x86-P166+ (133MHz)
1-2	1-2	2-3	1-2	2-3		AMD K5-PR100 (100MHz)
1-2	1-2	2-3	1-2	2-3		AMD K5-PR133 (100MHz)

3.9 电源连线 (P18,P19)

PIN	信号名称
1	电源正常
2	+5Vdc
3	+12Vdc
4	-12V dc
5	地
6	地
7	地
8	地
9	-5Vdc
10	+5Vdc
11	+5Vdc
12	+5Vdc

3.10 PS/2鼠标接口 (P22)

PIN	信号名称
1	+5Vdc
2	地
3	MDATA
4	MCLK

3.11 键盘接口 (KB1)

PIN	信号名称
1	键盘 时钟
2	键盘 信号
3	不用
4	地
5	VCC

Integrated IDE, Super I/O Subsystem

- ◆ IDE support
Chipset built-in PCI IDE support up to 4 IDE Drives
- ◆ On board I/O
One Floppy Port supporting 2 floppy drives of 360KB / 720KB / 1.44MB/ 2.88MB capacity.
Two serial ports (16550 Fast UART compatibles)
One parallel Port (Standard, ECP, EPP support)

PS/2 Mouse

- ◆ PS/2 Mouse
Supports PS/2 Mouse through a 1x4 header

Power Management

- ◆ Green functions
Support various Power Management schemes
Sleep Switch for power saving

BIOS Subsystem

- ◆ BIOS Shadowing
Shadow RAM for System and Video BIOS
- ◆ BIOS Features
Built-in setup, Power-on self test, Drive table optimization, User-definable drive types, Password protection, Shadowing options

Plug & Play / BIOS Update

- ◆ Plug & Play BIOS
Support Plug & Play for easy installation
- ◆ Flash EEPROM
Use Flash EEPROM (1M bits) to allow easy BIOS update

3. 接口联线

3.1 复位接口(P1)

PIN	信号名称
1	复位信号线
2	地

3.2 TURBO LED 接口(P2)

PIN	信号名称
1	Pull_Up_150
2	LED_Turbo-

3.3 扬声器接口(P3)

PIN	信号名称
1	数据输出
2	N.C.
3	地
4	+5Vdc

3.4 锁定接口(P4)

PIN	信号名称
1	+5Vdc
2	加锁信号
3	地
4	键盘初始化
5	地

1.2 Central Processing Unit

The Pentium processor is a superscalar, pipelined CPU that provides next generation performance for the existing PC compatible software.

The processor is equipped with an 8K code cache and an 8K data cache. Each cache is organized in a 2-way set-associative architecture, offering higher hit rates. The data cache can be configured in write-back or write-through modes.

The internal numeric coprocessor is redesigned to give three times the performance of the 80486 FPU. It is backward compatible with i486DX math coprocessor and complying to ANSI/IEEE standard 754-1985.

1.3 External Cache Subsystem

The external cache of RHINO 6VX is organized in a direct-mapped configuration with sizes of 256KB, or 512KB in write-back mode using synchronous SRAM (pipelined burst SRAM).

There are two options to support 256KB SRAM:

- (1) 256KB on board (2 pcs of 32Kx32 SRAM).

To support a total of 512KB SRAM, we should have:

- (1) 512KB on board (4 pcs of 32Kx32 SRAM).
- (2) 256KB on board and 256KB via cache module.

In addition, the presence and size of synchronous SRAM used is auto-detected by BIOS.

2. 安装及修改

2.1 RHINO 6VX的存储器配置表

BANK 2	BANK 1	Total
-----	512Kx32	4MB
-----	1Mx32	8MB
-----	2Mx32	16MB
-----	4Mx32	32MB
-----	8Mx32	64MB
512Kx32	-----	4MB
1Mx32	-----	8MB
2Mx32	-----	16MB
4Mx32	-----	32MB
8Mx32	-----	64MB
512Kx32	512Kx32	8MB
1Mx32	512Kx32	12MB
512Kx32	1Mx32	12MB
1Mx32	1Mx32	16MB
2Mx32	512Kx32	20MB
2Mx32	1Mx32	24MB
512Kx32	2Mx32	20MB
1Mx32	2Mx32	24MB
2Mx32	2Mx32	32MB
4Mx32	512Kx32	36MB
4Mx32	1Mx32	40MB
4Mx32	2Mx32	48MB
512Kx32	4Mx32	36MB
1Mx32	4Mx32	40MB
2Mx32	4Mx32	48MB
4Mx32	4Mx32	64MB
8Mx32	512Kx32	68MB
8Mx32	1Mx32	72MB
8Mx32	2Mx32	80MB
8Mx32	4Mx32	96MB
512Kx32	8Mx32	68MB
1Mx32	8Mx32	72MB
2Mx32	8Mx32	80MB
4Mx32	8Mx32	96MB
8Mx32	8Mx32	128MB

表二 存储器安装

1.7 Super I/O Subsystem

To facilitate system implementation, included in RHINO 6VX are two fast Enhanced IDE ports that can dramatically boost the system performance if fast IDE drives are used.

Furthermore, various formats floppy drives are also supported through the floppy connector on board. The motherboard is also equipped with two serial ports (16550 Fast UART compatibles) and one parallel port that operates in standard, ECP or EPP mode.

In addition, RHINO 6VX is designed to support the PS/2 mouse using specialized keyboard controller and the use of interrupt IRQ 12. Nevertheless, user can disable the PS/2 mouse function by means of jumpers.

1.8 Input/Output Subsystem

To allow greater system feasibility, RHINO 6VX has four ISA bus expansion connectors and three PCI expansion connectors. One of the expansion slots is shared by connectors that will accommodate either an ISA or a PCI expansion, but not both at the same time. Therefore, up to six expansion slots can be populated on RHINO 6VX. Furthermore, all the PCI slots can accept PCI bus master cards.

1.9 BIOS Subsystem

RHINO 6VX System BIOS is stored in Flash EEPROM (1 M bits) which allows easy upgrade through the utility found inside the diskette shipped with RHINO 6VX.

输入/输出子系统：

- ◆ PCI 总线插槽：2个32-BIT PCI 总线插槽
- ◆ ISA 总线插槽：3个16-BIT ISA 总线插槽
- ◆ 共享插槽：1个32-BIT PCI 或 16-BIT ISA 插槽
- ◆ I/O 总线速度：PCI 总线速度可高达33MHZ

集成IDE, 超级I/O子系统：

- ◆ IDE 接口：2个可提供多达4个 IDE 磁碟机的内设PCI IDE 接口
- ◆ I/O 接口：一个可支持两个软驱 (360K/ 720K/ 1.44M/ 2.88M) 的软驱接口, 两个串口, 一个并口

PS/2鼠标：

- ◆ PS/2 鼠标：支持PS/2 鼠标

电源管理：

- ◆ 环保功能：支持各种不同的电源管理方式, 睡眠开关可节省电耗.

BIOS 子系统：

- ◆ BIOS 影印：对系统及视频BIOS有专门的RAM 作影印
- ◆ BIOS 特征：具有设置, 通电自检, 驱动器表优化, 用户定义驱动器类型, 密码保护, 影印选项等功能

2.2 Fast Page mode / EDO DRAM Installation

There are four SIMM sockets located on the RHINO 6VX motherboard, marked BANK 1 and BANK 2. BANK 1 and BANK 2 are counted starting from right to left consecutively. Start to install the SIMM modules (IN PAIRS) from either Bank 1 or Bank 2. Depending on how your memory is configured, you may not need to use all the memory banks. Either x32 or x36 of 72 pins SIMM can be installed.

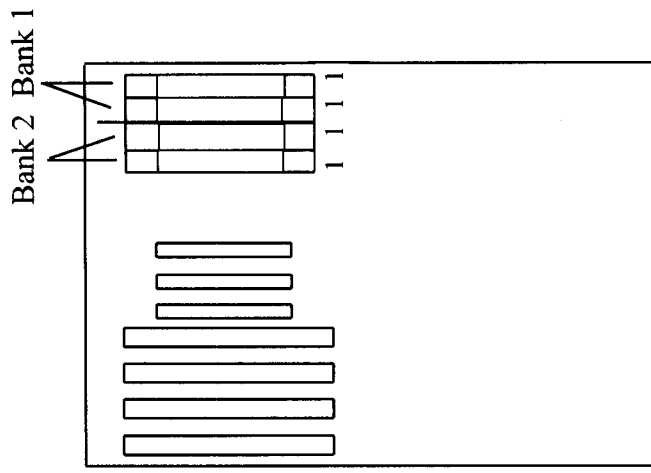


Figure 2 SIMM Sockets Location

2.3 Control of System Speed

System speed can be controlled by keyboard. To change the speed by keyboard, use the minus sign (-) and the plus sign (+). Press <control> + <alt> + <"-:"> for slow speed and <control> + <alt> + <"+"> for fast speed.

2.4 Reset CMOS

If the setting of the system setup is done improperly, it may make the system malfunction. If this happens, turn off the power and set jumper JP7 to 2-3 to clear the internal CMOS status register. Wait at least 5 seconds to ensure that the CMOS content has been completely cleared.

Next, set the jumper JP7 back to 1-2 and turn on the power. The BIOS will find the CMOS status register is reset and will regard the setup information invalid, so it will prompt you to correct the information.

B.3.3 Peripheral setup

PS/2 MOUSE support

	JP31	JP32	JP33
Enabled	1-2 *	2-3 *	2-3 *
Disabled	2-3	1-2	1-2

B.3.4 Miscellaneous

Power Good Signal select

	JP27
External Power Good	1-2 *
On-board Power Good	2-3

CMOS discharge

	JP7
Preserve CMOS	1-2 *
Clear CMOS	2-3

Battery select

	JP6
On-board Battery	1-2 *
External Battery	2-3

Reserved Jumpers

JP15	1-2
JP30	1-2

A.5 HD LED Connector (P5)

Pin	Signal Name
1	Pull Up 330
2	HD_LED-
3	HD_LED-
4	Pull Up 330

A.6 External Battery Connector (P9)

Pin	Signal Name
1	+3.6Vdc
2	N.C.
3	Ground
4	Ground

A.7 Sleep Switch (P10)

Pin	Signal Name
1	EPMI
2	Ground

A.8 USB Connector (P24)

Pin	Signal Name	Pin	Signal Name
6	VCC	1	VCC
7	Port 1-	2	Port 0-
8	Port 1+	3	Port 0+
9	Ground	4	Ground
10	NC	5	NC

APPENDIX-B

HARDWARE SETTINGS

CPU Type

JP4	JP5	JP8	JP9	JP10	CPU Clock	CPU TYPE
1-2	2-3	2-3	2-3	1-2	50MHz	Intel P54C-75
2-3	1-2	2-3	2-3	1-2	50MHz	Cyrix 6x86-P120+ (100MHz)
1-2	1-2	2-3	2-3	1-2	55MHz	AMD K5-PR75
2-3	1-2	1-2	1-2	1-2	55MHz	Cyrix 6x86-P133+ (110MHz)
1-2	1-2	1-2	2-3	2-3	60MHz	Intel P54C-90
2-3	1-2	1-2	2-3	2-3	60MHz	Intel P54C-120
2-3	2-3	1-2	2-3	2-3	60MHz	Intel P54C-150
1-2	2-3	1-2	2-3	2-3	60MHz	Intel P54C-180
2-3	1-2	1-2	2-3	2-3	60MHz	Cyrix 6x86-P150+ (120MHz)
1-2	1-2	1-2	2-3	2-3	60MHz	AMD K5-PR90
1-2	1-2	1-2	2-3	2-3	60MHz	AMD K5-PR120 (90MHz)
1-2	1-2	1-2	2-3	2-3	60MHz	AMD K5-PR150 (120MHz)
2-3	1-2	1-2	2-3	2-3	60MHz	AMD K5-PR150 (120MHz)
1-2	1-2	2-3	1-2	2-3	66MHz	Intel P54C-100
2-3	1-2	2-3	1-2	2-3	66MHz	Intel P54C-133
2-3	2-3	2-3	1-2	2-3	66MHz	Intel P54C-166
1-2	2-3	2-3	1-2	2-3	66MHz	Intel P54C-200
2-3	1-2	2-3	1-2	2-3	66MHz	Cyrix 6x86-P166+ (133MHz)
1-2	1-2	2-3	1-2	2-3	66MHz	AMD K5-PR100
1-2	1-2	2-3	1-2	2-3	66MHz	AMD K5-PR133 (100MHz)

B.3.2 External cache (L2 cache) setting

Synchronous SRAM

256K Configuration :

1. 256K cache using on board 256K SRAM

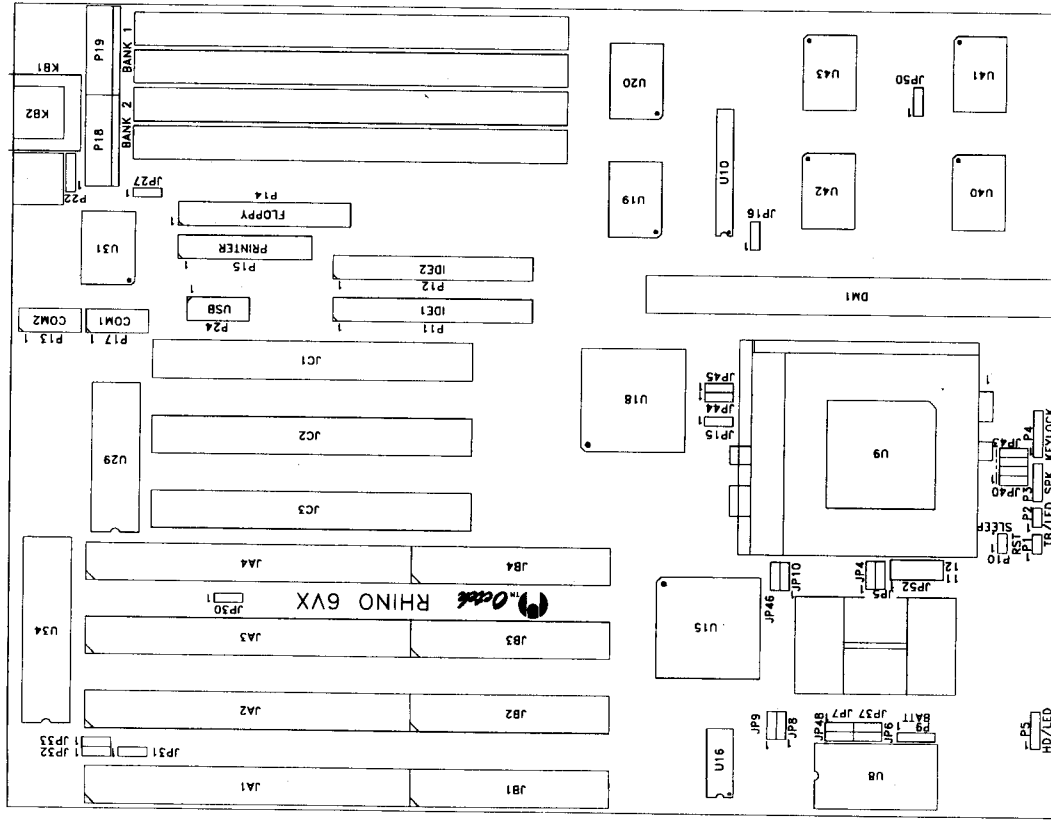
SRAM	Location	Type	Speed	Voltage
Tag SRAM	U10	8Kx8 / 32Kx8	15ns	5V I/O
Data SRAM	U41, U43	2 pcs 32Kx32 Pipelined Burst SRAM	7ns (Clock to o/p valid)	3.3V I/O

JP16*	JP50*
OPEN	2-3

B.1 System Component Map

Jumper Connectors	Function
P1	Reset
P2	Turbo LED
P3	Speaker
P4	Keypress
P5	IDE LED Connector
P9	External Battery Connector
P10	Sleep Connector
P11	Primary IDE Connector
P12	Secondary IDE Connector
P13	Serial Port 2
P14	Floppy Connector
P15	Printer Port Connector
P17	Serial Port 1
P18	Power Connector
P19	Power Connector
P22	PS/2 Mouse Connector
P24	USB Connector
KB1	Keyboard Connector

B.2 Layout of RHINO 6VX Main Board



B.3 Jumper Settings

All factory settings are marked by * in the following sections.

B.3.1 CPU related settings

CPU Voltage Core Selection

RHINO 6VX has on board voltage regulators support Intel Pentium CPU such as P54C, P54CQS, P54CS, Cyrix 6x86 and AMD K5 CPU. The voltage selection for Core voltage is done by JP52 as follows :

JP52	CPU Core voltage	CPU Type
1-2	3.5V(VRE)	Cyrix 6x86, AMD K5
3-4 *	3.3V	Intel P54C, P54CQS, P54CS

NOTE : Be careful to select the appropriate Core voltage for different CPU. Improper Core voltage supplied to CPU may result in "PERMANENT DAMAGE" to CPU !

A.9 Power Connector (P18,P19)

Pin	Signal Name
1	Power Good
2	+5Vdc
3	+12Vdc
4	-12V dc
5	Ground
6	Ground
7	Ground
8	Ground
9	-5Vdc
10	+5Vdc
11	+5Vdc
12	+5Vdc

A.10 PS/2 Mouse Connector (P22)

Pin	Signal Name
1	+5V dc
2	GND
3	MDATA
4	MCLK

A.11 Keyboard Connector (KB1)

Pin	Signal Name
1	Keyboard clock
2	Keyboard data
3	Not used
4	Ground
5	VCC

512K Configuration :

1. 512K cache using On board 512K SRAM (4pcs PB SRAM)

SRAM	Location	Type	Speed	Voltage
Tag SRAM	U10	32Kx8	15ns	5V I/O
Data SRAM	U40, U41, U42, U43	4 pcs 32Kx32 Pipelined Burst SRAM	7ns (Clock to o/p valid)	3.3V I/O

JP16	JP50
2-3	1-2

2. 512K cache using on board 256K and 256K Cache Module w/o Tag SRAM

SRAM	Location	Type	Speed	Voltage
Tag SRAM	U10	32Kx8	15ns	5V I/O
Data SRAM (1 st 256KB)	U41, U43	2 pcs of 32Kx32 pipelined burst SRAM	7ns (Clock to o/p valid)	3.3V I/O
Data RAM (2 nd 256KB)	DM1	256K Cache Module w/o Tag	7ns (Clock to o/p valid)	3.3V I/O

JP16	JP50
2-3	1-2

APPENDIX-A

CONNECTORS PINOUT

A.1 Reset Connector (P1)

Pin	Signal Name
1	Reset
2	Ground

A.2 Turbo LED Connector (P2)

Pin	Signal Name
1	Pull_Up_150
2	LED_Turbo-

A.3 Speaker Connector (P3)

Pin	Signal Name
1	Speaker Data_Out
2	N.C.
3	Ground
4	+5Vdc

A.4 Keylock Connector (P4)

Pin	Signal Name
1	+5Vdc
2	Mechanical Key
3	Ground
4	Keyboard Inhibit
5	Ground

目录

1. 综述.....	1
2. 安装及修改.....	4
2.1 RHINO 6VX 的存储器配置表.....	4
2.2 系统速度控制.....	5
2.3 CMOS复位.....	5
3. 接口联线.....	6
3.1 复位接口(P1).....	6
3.2 TURBO LED 接口(P2).....	6
3.3 扬声器接口(P3).....	6
3.4 锁定接口(P4).....	6
3.5 硬盘 LED接口(P5).....	7
3.6 外接电池接口(P9).....	7
3.7 睡眠开关(P10).....	7
3.8 USB 接口(P24).....	7
3.9 电源连线 (P18,P19).....	8
3.10 PS/2鼠标接口(P22).....	8
3.11 键盘接口(KB1).....	8
4. 硬件设置.....	9
4.1 系统元件图.....	9
4.2 跳线设置.....	10

Below is a memory configuration table for RHINO 6VX.

BANK 2	BANK 1	Total
-----	512Kx32	4MB
-----	1Mx32	8MB
-----	2Mx32	16MB
-----	4Mx32	32MB
-----	8Mx32	64MB
512Kx32	-----	4MB
1Mx32	-----	8MB
2Mx32	-----	16MB
4Mx32	-----	32MB
8Mx32	-----	64MB
512Kx32	512Kx32	8MB
1Mx32	512Kx32	12MB
512Kx32	1Mx32	12MB
1Mx32	1Mx32	16MB
2Mx32	512Kx32	20MB
2Mx32	1Mx32	24MB
512Kx32	2Mx32	20MB
1Mx32	2Mx32	24MB
2Mx32	2Mx32	32MB
4Mx32	512Kx32	36MB
4Mx32	1Mx32	40MB
4Mx32	2Mx32	48MB
512Kx32	4Mx32	36MB
1Mx32	4Mx32	40MB
2Mx32	4Mx32	48MB
4Mx32	4Mx32	64MB
8Mx32	512Kx32	68MB
8Mx32	1Mx32	72MB
8Mx32	2Mx32	80MB
8Mx32	4Mx32	96MB
512Kx32	8Mx32	68MB
1Mx32	8Mx32	72MB
2Mx32	8Mx32	80MB
4Mx32	8Mx32	96MB
8Mx32	8Mx32	128MB

1. 综述

处理器:

- 处理器类型: Intel 奔腾 CPU 包括 P54C, P54CQS, P54CS, AMD K5 以及 Cyrix 6x86 CPU
- CPU 外部时钟: 50/55/60/66MHz

芯片:

- 主板芯片: Intel 82430VX
- 超级 I/O 芯片: 665/669 超级 I/O 芯片

高速缓存:

- 内部缓存: 8KB 数据缓存, 8KB 代码缓存
- 外部缓存: 256/512KB Sync. Pipelined Burst SRAM

存储器子系统:

- DRAM SIMM 插槽: 4 x 72 脚 4MB/ 8MB/ 16MB/ 32MB DRAM 模块
- 最大存储容量: 128MB
- DRAM 类型: 快速页模式或EDO DRAM
- 增强功能: 可同时支持快速页模式及EDO DRAM

Table 1 Memory Configuration Table

CHAPTER 2

INSTALLATION AND UPGRADE

2.1 CPU Installation

The CPU is composed of pins that can easily be bent during installation, causing permanent damage to the processor. It is therefore very important that you make sure the pins are straight before installing the CPU onto the SPGA socket located on RHINO 6VX (refer to layout for exact location). To properly align the CPU with the socket, align pin 1 of the CPU (with a notch at the corner) with pin 1 of the CPU socket as demonstrated below.

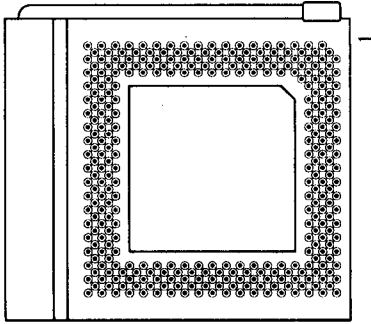


Figure 1 Socket 7 for Pentium CPU

USB 设备:

- 通用串行线设备:

联接主板与中枢控制的介面
2个可编程接口

即插即用/BIOS更新:

- 即插即用BIOS:
- 电可擦EEPROM:

支持即插即用, 使安装更简单
使用电可擦EEPROM (1M BIT) 使得BIOS的更新更加容易

系统支持功能:

- 系统功能:
- 支持功能:
- 时钟:

7个DMA通道, 16级中断, 可编程计时器
快速A20门电路及快速复位
增强型时钟及日历, 同时具有
电池备份

其它特性:

- 电源正常:
- 3.3V供电:

主板可产生电源正常信号
主板具供电 (3.3V) 功能, 供给
3.3V器件如CPU, SRAM等使用。
最大功耗为30W

- 开关:

复位开关, 键盘锁定开关及睡眠开关

- 大小:

8.5 (宽) X 11 (长)

1.4 DRAM Subsystem

The main memory in RHINO 6VX is organized as a 64-bit memory pool. Both fast-page mode and EDO DRAMs are supported.

EDO DRAM stands for Extended Data Out DRAM and is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge, unlike standard fast page mode DRAM which tri-states the memory data when CAS# is deasserted to precharge for the next cycle. As a result, the CAS# precharge can now overlap with the data valid time to allow CAS# to negate earlier while still satisfying the memory data valid window time.

In addition, mix of EDO/ Fast Page Mode DRAM could be used on RHINO 6VX. The presence of EDO/ Fast Page Mode DRAM is auto-detected by BIOS without any related jumper setting.

1.5 PCI Bus

The Peripheral Component Interconnect (PCI) local bus was specified to establish a high performance local bus standard. It is a 32-bit wide bus supporting burst transactions

The PCI local bus implemented in RHINO 6VX is fully compliant to v2.1 specification. Up to four PCI bus masters are supported.

1.6 Universal Serial Bus

The Universal Serial Bus (USB) is a cable bus that supports data exchange between a host computer and a wide range of simultaneously accessible peripherals.

2.2 系统速度控制:

系统速度可以通过键盘. 使用减号(-)或加号(+)来控制. 按 <Control> + <alt> + <-> 减低速度, 按 <control>+<alt>+<+>增加速度.

2.3 CMOS复位:

如果系统设置不正确, 可能会导致系统失灵. 如果出现这种情况, 先关电源, 再将跳线JP7跳至2-3, 这样CMOS的状态寄存器会备清除. 等待至少5秒钟, 以保证CMOS中的内容被清除. 然后将跳线跳回1-2并通电. BIOS会发现CMOS状态寄存器被复位并认为设置信息错误, 并提示你更改设置信息.

USB Devices

- ◆ USB Devices
Interfaced with both host and hub control functions
2 programmable USB ports

System Support Functions

- ◆ System functions
7 DMA channels, 16 level interrupts, Programmable timers
- ◆ Support functions
Fast A20 gate and Fast Reset
- ◆ Clock
Enhanced real time clock/calendar with battery back-up

Other Features

- ◆ Power good
On board power good signal generation
- ◆ 3.3V supply
On board 3.3V supply to eliminate the need for special power supply for 3.3V component e.g. CPU, SRAM. Maximum rating : 30 W.
- ◆ Switches
Reset, Keylock switches, Sleep Switch.
- ◆ Size
8.5" (W) x 11" (L)

3.5 硬盘 LED接口(P5)

PIN	信号名称
1	PULL_UP_330
2	HD_LED-
3	HD_LED-
4	Pull_Up_330

3.6 外接电池接口(P9)

PIN	信号名称
1	+3.6Vdc
2	N.C.
3	地
4	地

3.7 睡眠开关(P10)

PIN	信号名称
1	EPMI
2	地

3.8 USB 接口(P24)

PIN	信号名称	PIN	信号名称
6	VCC	1	VCC
7	Port 1-	2	Port 0-
8	Port 1+	3	Port 0+
9	地	4	地
10	NC	5	NC

1.1 General Specifications Overview

Processor:

- ◆ Processor Type Intel Pentium CPU including P54C, P54CQS, P54CS, AMD K5 and Cyrix 6x86 CPU.
- ◆ External CPU clock 50/55/60/66 MHz

Chipset:

- ◆ Motherboard chipset Intel 82430VX
- ◆ Super I/O chipset 665/669 super I/O chipset

Cache Architecture:

- ◆ Internal Cache 8KB data cache
- ◆ External Cache 8KB code cache
256/512KB Synchronous Pipelined Burst SRAM

Memory Subsystem:

- ◆ DRAM SIMM sockets 4 x 72 pin 4MB / 8MB / 16MB / 32MB DRAM modules
- ◆ Max. Memory Size 128MB
- ◆ DRAM Type Fast Page Mode or EDO DRAM
- ◆ Enhancement Mix of Fast Page Mode or EDO DRAM supported

Input/Output Subsystem

- ◆ PCI bus slots 2 x 32-bit PCI Bus slots (3 masters)
- ◆ ISA bus slots 3 x 16-bit ISA slots
- ◆ shared bus slots 1 x 32 bit PCI bus slot (master) OR 1 x 16-bit ISA slot
- ◆ I/O bus speed Up to 33MHz (PCI bus)

4. 硬件设置

4.1 系统元件图

接口标识	功能
P1	连接复位开关
P2	连接 Turbo LED
P3	连接扬声器
P4	连接锁定装置
P5	连接 IDE LED
P9	连接外部电源
P10	连接睡眠开关
P11	连接第一 IDE
P12	连接第二 IDE
P13	连接串口 2
P14	连接软驱
P15	连接打印口
P17	连接串口 1
P18	连接电源
P19	连接电源
P22	连接 PS/2 鼠标
P24	连接 USB
KB1	连接键盘

A.9	Power Connector (P18,P19).....	14
A.10	PS/2 Mouse Connector (P22).....	14
A.11	Keyboard Connector (KB1)	14

Appendix-B: Hardware Settings

B.1	System Component Map	15
B.2	Layout of RHINO 6VX Main Board	16
B.3	Jumper Settings	17
B.3.1	CPU related settings	17
B.3.2	External cache (L2 cache) setting.....	18
B.3.3	Peripheral setup	20
B.3.4	Miscellaneous	20

4.2.2 外部缓存有关设置

同步缓存

256K 配置:

1. 256KB 缓存使用主板上的256K SRAM

SRAM	位置	类型	速度	电压
Tag SRAM	U10	8Kx8 / 32Kx8	15ns	5V I/O
Data SRAM	U41,U43	2 片 32Kx32 Pipelined Burst SRAM	7ns (Clock to o/p valid)	3.3V I/O

JP16*	JP50*
OPEN	2-3

512K 配置:

1. 512K缓存使用主板上的 512K SRAM (4 片 PB SRAM)

SRAM	位置	类型	速度	电压
Tag SRAM	U10	32Kx8	15ns	5V I/O
Data SRAM	U40, U41, U42, U43	4 片 32Kx32 Pipelined Burst SRAM	7ns (Clock to o/p valid)	3.3V I/O

JP16	JP50
2-3	1-2

4.2.4 其它设置

电源正常信号选择

	JP27
外部电源正常	1-2 *
主板电源正常	2-3

CMOS 放电

	JP7
CMOS 保护	1-2 *
CMOS 清除	2-3

电池选择

	JP6
主板电源	1-2 *
外部电源	2-3

保留跳线

JP15	1-2
JP30	1-2